REMARKS

Claims 1-40 are pending in the application. Claims 1, 2, 21 and 29 have been amended. Support for the amendments may be found within the entirety of the specification, and particularly at pages 2-6 and 10-14. No new matter has been added by these amendments.

Claims 4, 7-12, 17-20, 24, 27-32 and 37-40 have been objected to as being dependent on a rejected claim, but have been otherwise deemed to include allowable subject matter. Applicants thank the Examiner for consideration and recognition of the allowability of these claims.

Claims 1-3, 5, 6, 13-16, 21-23, 25, 26, and 33-36 have been rejected under 35 U.S.C. § 102(b) as being obvious over U.S. Patent No. 5,677,917 to Wheelus *et al.* in view of U.S. Patent No. 4,653,051 to Sugimura *et al.* Applicants respectfully request favorable consideration and earnestly solicit allowance of the application in light of the amendments and following remarks.

Independent claim 1

Independent claim 1 is directed to a memory having, *inter alia*, a plurality of replacement storage elements and a plurality of address fuse units that each store a replacement address identifying one of the storage elements to be replaced by a replacement storage element. The replacement addresses each form a respective row or column of a fuse array "having 2^m bit rows and 2^n bit columns." A vector generator produces "a 2^n bit row

vector based on the rows of the fuse array" and "a 2^m bit column vector based on the columns of the fuse array."

Applicants respectfully submit that the cited combination of Wheelus and Sugimura fails to disclose or suggest the limitations of independent claim 1. Wheelus is directed to a memory that includes programmable fuses coupled to scannable flip-flops and used to program specific information such as repair (redundancy) information. (Abstract; col. 2, ll. 7-12; col. 5, ll. 34-49). The memory of Wheelus includes a fuse circuit array having row fuses organized in N-rows and column fuses organized in M-columns. (Figure 4; col. 6, ll. 33-34; col. 8, ll. 48-50). The fuse circuit has input terminals to receive N bit address (INQ1-INQN). The output of the memory array includes M bit output signal FUSE LINE 1 to FUSE LINE M. (Figure 4; col. 6, ll. 40-45). Sugimura relates to an apparatus for detecting and correcting errors on product codes suitable for parity checking in digital information data transmission or recording. (Abstract; col. 1, ll. 7-12). The code is arranged in a (k x 1) matrix. (col. 1, ll. 59-65; col. 2, ll. 49-51).

The cited combination of Wheelus and Sugimura fails to describe or suggest "a vector generator operable to produce a 2^n bit row vector based on the 2^m bit rows of the fuse array and to produce a 2^m bit column vector based on the 2^n bit columns of the fuse array, as recited in amended independent claim 1. To the contrary, Wheelus discloses a N x M fuse circuit array that is addressed by an N-bit word (INQ1 to INQN) to produce an M-bit output (FUSE LINE 1 to FUSE LINE M). Whereas Wheelus provides an output based on the columns of the fuse array, the vector generator of claim 1 is operable to produce a row vector

based on the 2^m bit rows. The vector generator of claim 1 is also operable to produce a column vector based on the 2^n bit columns. Neither Wheelus nor Sugimura disclose or suggest such a vector generator. Accordingly, Applicants respectfully submit that amended independent claim 1 would not have been obvious.

Furthermore, Applicants respectfully submit that a person having skill in the art would not be motivated to combine the cited references. In particular, Wheelus relates to a memory array having programmable fuses and scannable flip-flops that are used to program predetermined information about the integrated circuit, such as information that may be used during or after package testing. (col. 2, ll. 7-15). The memory of Wheelus is used during a testing procedure to identify which memory elements have been repaired. (col. 2, ll. 16-22). Sugimura, on the other hand, relates to correcting errors. (col. 2, ll. 3-14). Since any errors in the Wheelus memory have been corrected, a person of ordinary skill would not be motivated to combine Sugimura with Wheelus.

Notwithstanding the same, had one having skill in the art combined Sugimura with Wheelus, the combination would relate to producing a checksum of the fuses of the respective rows of a fuse array and would include a further checksum element in each row of the fuse array. Since neither Wheelus nor Sugimura disclose or suggest producing a row or column vector as recited by amended independent claim 1, the cited combination also does not disclose or suggest a "compression unit operable to produce a row checksum from the row vector and to produce a column checksum from the column vector, as recite by claim 1. Therefore, the Wheelus and Sugimura combination does not disclose or suggest the

limitations of amended independent claim 1. Accordingly, Applicants respectfully request reconsideration of the rejection of claim 1.

Independent claim 21

Independent claim 21 is directed to a method including forming a fuse array from a plurality of replacement addresses, each identifying one of a plurality of storage elements of a memory array to be replaced by a replacement storage element. Each replacement address forms "a respective row or column of the fuse array having 2^m bit rows and 2^n bit columns." A 2^n bit row vector is produced based on the 2^m bit rows of the fuse array and a 2^m bit column vector is produced based on the 2^n bit columns of the fuse array. Finally a row checksum is produced from the row vector, and a column checksum is produced from the column vector.

Applicants respectfully submit that the cited combination of Wheelus and Sugimura fails to disclose all the limitations of independent claim 21. As discussed, the Wheelus and Sugimura combination fails to describe or suggest "producing a 2^n bit row vector based on the 2^m bit rows of the fuse array" and "producing a 2^m bit column vector based on the 2^n bit columns of the fuse array," as recited in amended independent claim 21. Accordingly, Applicants respectfully submit that amended independent claim 21 would not have been obvious.

In addition, a person having skill in the art would not be motivated to combine Sugimura with Wheelus because Wheelus relates to a memory having information that is used during a testing procedure to identify which memory elements have been repaired, (col. 2, ll. 16-22), and Sugimura, on the other hand, relates to correcting errors. (col. 2, ll. 3-14). Since any errors in the Wheelus memory have been corrected, a person of ordinary skill would not be motivated to combine Sugimura with Wheelus. Indeed, since neither Wheelus

nor Sugimura disclose or suggest producing a row or column vector as recited by amended independent claim 21, the cited combination also does not disclose or suggest "producing a row checksum from the row vector" or "producing a column checksum from the column vector," as recite by claim 21. Therefore, the Wheelus and Sugimura combination does not disclose or suggest the limitations of amended independent claim 21. Accordingly, Applicants respectfully request reconsideration of the rejection of claim 21.

Dependent Claims

For similar reasons, the Wheelus and Sugimura cited combination also fails to disclose or suggest the limitations of claims 2-20 and 22-40. As discussed above, the Wheelus and Sugimura combination does not disclose or suggest the limitations of independent claims 1 and 21, and therefore, the combination also does not disclose or suggest the limitations for claims dependent therefrom. Claims 2 and 29 have been amended to correct minor typographical errors. Accordingly, applicant also respectfully request favorable consideration of claims 2-20 and 22-40.

CONCLUSION

In view of the foregoing amendments and reasons, Applicant respectfully requests favorable consideration and earnestly solicits allowance of all pending claims. Any inquiries regarding this communication may be directed to the undersigned attorney at the telephone number listed below.

Respectfully submitted,

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